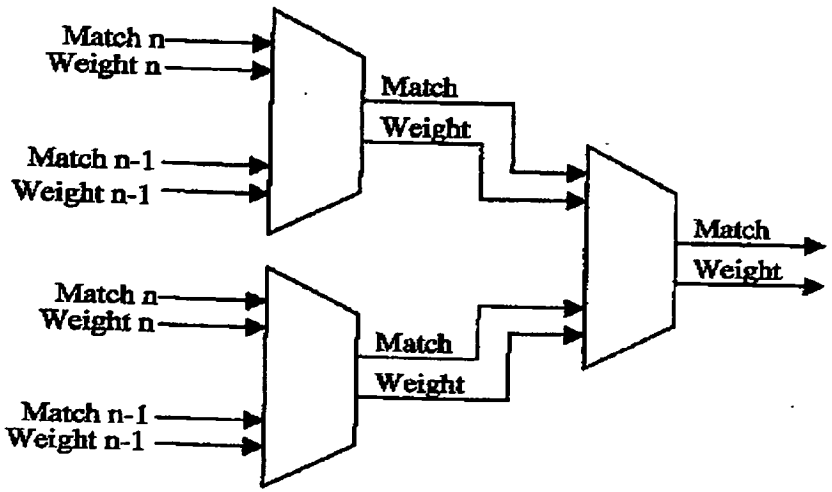
Improved Match Resolution Circuit for Content Addressable Memory (CAM)

- Weight based, multiple CAM entry match resolution
  - A Match Weight can be stored as part of a CAM word
  - When multiple matches occur in a CAM the "Best Match" can be determined by an arithmetic or logical comparison of the Match Weights of all matching CAM entries.
- Circuit provides for hierarchical match resolution. If two or more entries have the same weight according to one criteria, a second match resolution criteria can be applied to these entries.
- Weight can comprise any of the following:
  - Weight field stored in the CAM array or associated data.
  - Length of the longest contiguous unmasked field in the CAM entry (Improved implementation of longest match).
  - Total number of unmasked bits in the CAM entry.
  - Total Number of matching bits resulting from a compare (Improved implementation of best match).
  - Position in the CAM array.

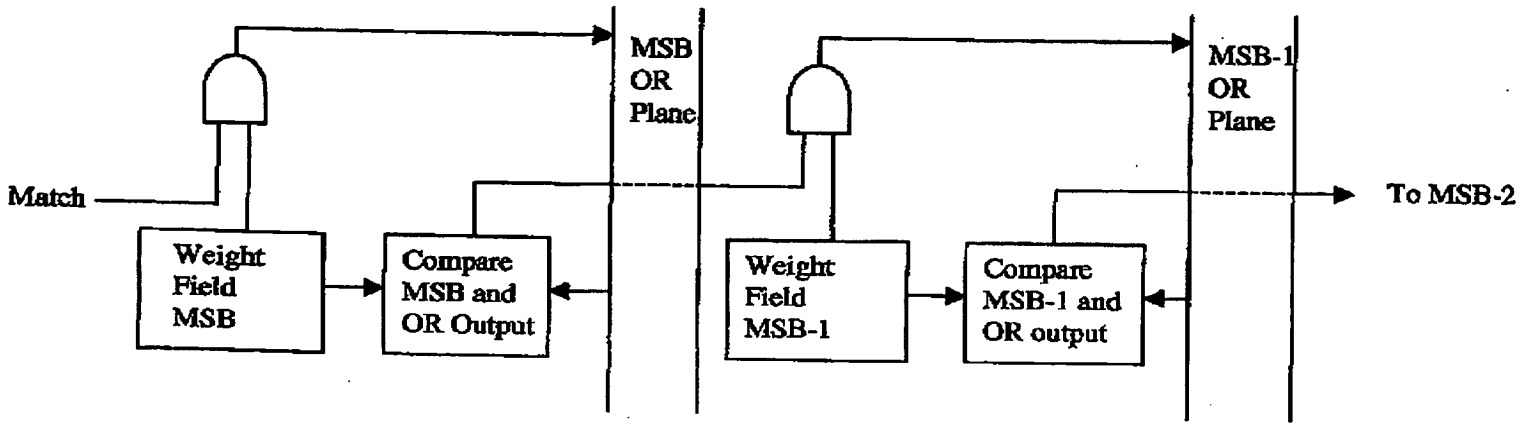
Match Resolution Theory

- CAM Match resolution can be described as the process of finding the CAM entry with the highest weight.
- Match resolution can be implemented as a stack of two entry match resolution circuits where each two entry match resolution circuit compares two input values and outputs the greater value. The match signal is simply treated as the high order bit of the weight.
- If weight is the position in the CAM array this if functionally equivalent to the conventional use of a priority encoder.



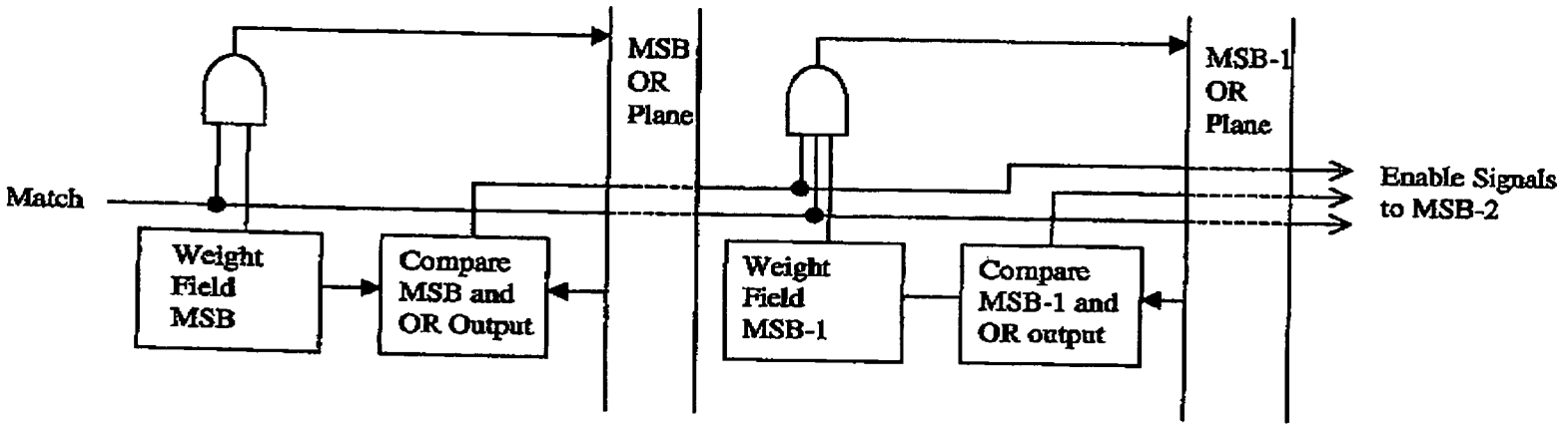
Match Resolution Implementation

- Weight based match resolution can be implemented using a bit slice approach to a distributed compare.
- The MSB of the weights of all matching CAM words are ORed together.
- The Most Significant Bit (MSB) of all weight fields are compared to the result of the OR. If the weight field bit matches the result a compare OK signal is propagated to the next less significant bit.
- All of the bits match for the highest priority CAM word.



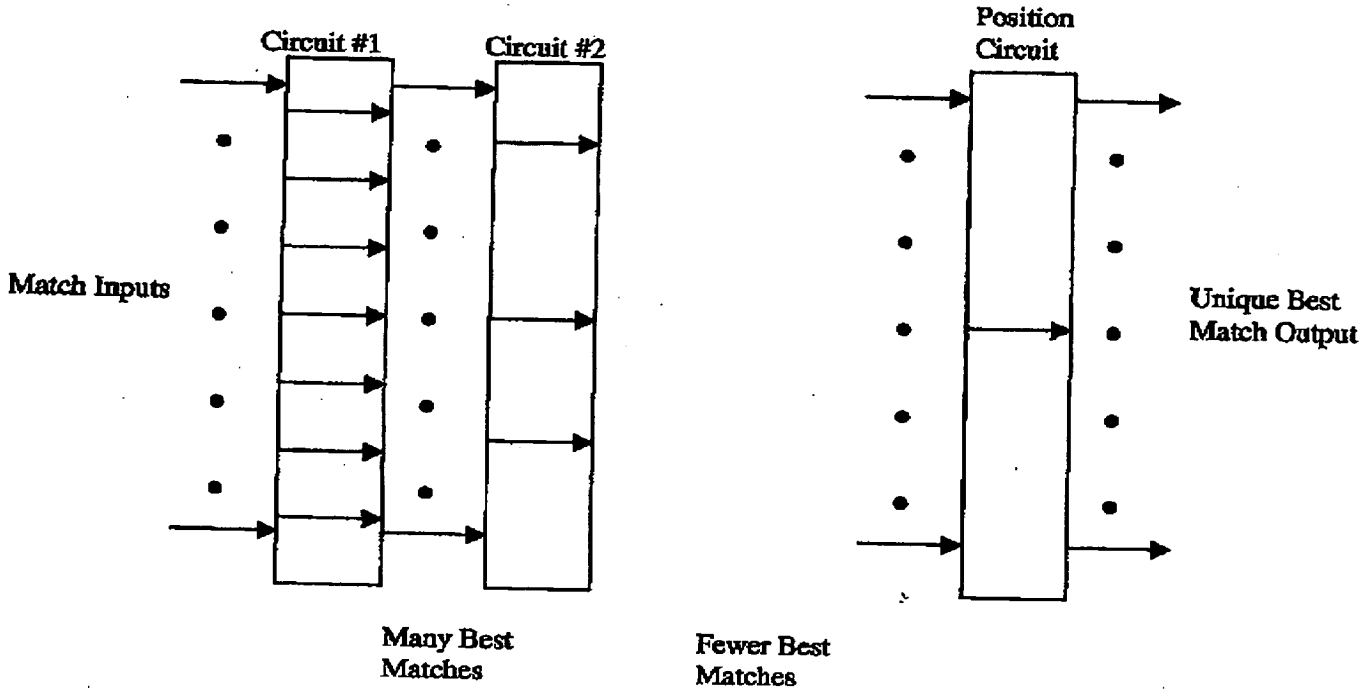
Higher Speed Match Resolution and OR Plane Implementation

- Match resolution speed can be improved by adding "Look Ahead" logic similar to a adder circuit.
- The or plane can also be implemented using the wide gate structures developed for our CAM.



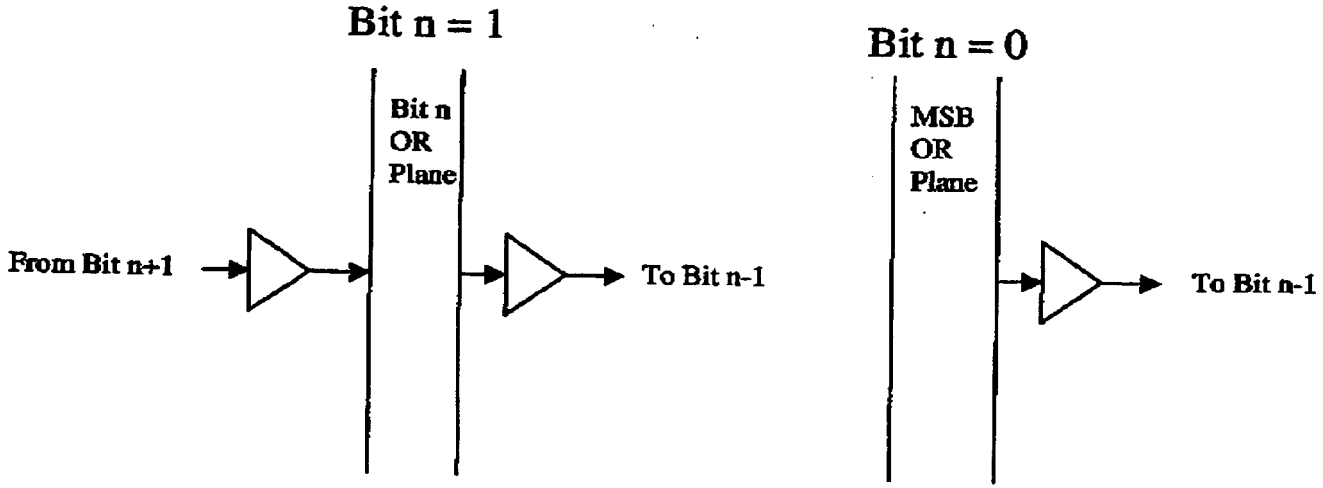
Best Match based on Multiple Criteria

- Two or more match resolution circuits can be cascaded such that if there are multiple "best" matches based on a first criterion (e.g. network path length) a second criterion (e.g. link speed) can be used to determine the best match.
- To assure a unique "best" match array position can be used as a final criterion.



Array Position as a Special Case

- When array position is used as the weight the driver and the associated portion of the OR function of the match circuit can be removed for bits with a weight of zero (a zero if the only input that can be presented to the OR).
- This same logic can be replaced by a buffer for bits with a weight of one.
- The compare function for these bits is simply a buffer.



Alternate Implementation for Array Position Based Best Match

- Implementation below resolves multiple matches based on array position and outputs address of highest matching entry.

Alternate Implementation for Array Position Based Best Match Operation

- The match signals from the CAM Array are divided into two sub-groups, High priority and low priority.
- An OR function (can be a wired OR) is used to determine if any high priority match has occurred.
- Each sub-group is then divided into two smaller sub-sub-groups the match signals of the higher priority sub-sub-group of the low priority sub-group are ANDed with the complement of the output of the high priority OR (higher priority match disables lower priority outputs to OR)
- Division into sub-groups and AND/OR combinations continues until individual pairs of match lines are processed
- Output of ORs it the complement of the address of the highest position match.

Match Queue Improvements

- Classical CAMs, multi-ported CAMs, re-configurable CAMs and CAMs with best match/longest match functions can all be enhanced by the inclusion of a Match Queue.
- Match Queue is used in addition to any of the prior art multiple match resolution methods or our Improved Match Resolution Circuit.
- Associated data for all entries that match an input value and meet the match resolution criteria (highest weight) are loaded into a FIFO memory in priority order according to a second criteria (typically array position).